IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Richard C. Foss, Peter B. Gillingham and Graham Allan		
Application No.:	10/645,330	Group Art Unit:	2818
Filed:	August 21, 2003	Examiner:	Michael T. Tran
Confirmation No.:	7565		
Title:	DELAYED LOCKED LOOP IMPLEMENTATION IN A SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY		

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or is being facsimile transmitted to the United States Patent and Trademark Office on:

8/23/04 Jennifer A. Tardiff
Date Signature

Jennifer A. Tardiff
Typed or printed name of person signing certificate

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Information Disclosure Statement is submitted under 37 CFR 1.97(c) with a $180.00 fee under 37 CFR 1.17(p).

Attached are the contentions of a Defendant, Infineon, with respect to patent 6,067,272 to which this application claims priority. Previously uncited references cited in those contentions, additional references cited by a potential licensee and yet additional references noted by Applicant are cited herein, although not all are considered to be prior art.

Enclosed herewith is Form PTO-1449, and copies of all foreign patent documents and other documents are attached. Since this application was filed after June 30, 2003, copies of issued U.S. patents and published U.S. applications are not required and are not being provided.

It is requested that the information disclosed herein be made of record in this application.

Please charge any deficiency in fees and credit any overpayment to Deposit Account 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By _____

James M. Smith
Registration No.: 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Dated: 8/20/4

PTO-1449 REPRODUCED	ATTORNEY DOCKET NO.	APPLICATION NO.	
SUPPLEMENTAL INFORMATION DISCLOSURE CITATION IN AN APPLICATION	2037.1004-007	10/645,330	
	FIRST NAMED INVENTOR	FILING DATE	
August 18, 2004	Richard C. Foss	August 21, 2003	
(Use several sheets if necessary)	EXAMINER	CONFIRMATION NO.	GROUP
	Michael T. Tran	7565	2818

		OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*
	AV	Hatakeyama, Atsushi, et al., "A 256Mb SDRAM Using a Register-Controlled Digital DLL," Fujitsu Limited, Kawasaki, Japan.
	AW	Hatakeyama, Atsushi, et al., "A 256-Mb SDRAM Using a Register-Controlled Digital DLL," *IEEE Journal of Solid-State Circuits,* Vol. 32, No. 11, pp. 1728-1734 (November 1997).
	AX	Efendovich, Avner, et al., "Multifrequency Zero-Jitter Delay-Locked Loop," *IEEE Journal of Solid-State Circuits,* Vol. 29, No. 1, pp. 67-70 (January 1994).
	AY	Choi, Yunho, et al., "16Mbit Synchronous DRAM with 125Mbyte/sec Data Rate," 1993 Symposium on VLSI Circuits Digest of Technical Papers, pp. 65-66, (1993).
	AZ	Lee, Thomas H., et al., "A 2.5V Delay-Locked Loop for an 18Mb 500MB/s DRAM," IEEE International Solid-State Circuits Conference, Session 18, pp. 300-301 (February 18, 1994).
	AR2	Takai, Yasuhiro, et al., "250 Mbyte/s Synchronous DRAM Using a 3-Stage-Pipelined Architecture," *IEEE Journal of Solid-State Circuits,* Vol. 29, No. 4, pp. 426-431 (April 1994).
	AS2	Choi, Yunho, et al., "16-Mb Synchronous DRAM with 125-Mbyte/s Data Rate," *IEEE Journal of Solid-State Circuits,* Vol. 29, No. 4, pp. 529-533 (April 1994).
	AT2	Takai, Y., et al., "250 Mbyte/sec Synchronous DRAM Using a 3-Stage-Pipelined Architecture,"1993 Symposium on VLSI Circuits Digest of Technical Papers, pp. 59-60, (1993).

EXAMINER	DATE CONSIDERED

PTO-1449 REPRODUCED	ATTORNEY DOCKET NO.	APPLICATION NO.	
SUPPLEMENTAL INFORMATION DISCLOSURE CITATION IN AN APPLICATION	2037.1004-007	10/645,330	
	FIRST NAMED INVENTOR	FILING DATE	
August 18, 2004	Richard C. Foss	August 21, 2003	
(Use several sheets if necessary)	EXAMINER	CONFIRMATION NO.	GROUP
	Michael T. Tran	7565	2818

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	REF. NO.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
	AC2	4,623,805	11-18-1986	Flora et al.
	AD2	4,755,704	07-05-1988	Flora et al.
	AE2	4,338,569	07-06-1982	Petrich
	AF2	4,604,582	08-05-1986	Strenkowski et al.
	AG2	4,637,018	01-13-1987	Flora et al.
	AH2	5,272,729	12-21-1993	Bechade et al.
	AI2	4,330,852	05-18-1982	Redwine et al.

OIPE AUG 26 2004 PATENT & TRADEMARK

EXAMINER	DATE CONSIDERED